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PATENT ABSTRACTS OF JAPAN(21) Application number: **54131483**(51) Intl. Cl.: **H01L 23/52 H01L 27/04**(22) Application date: **11.10.79**

<p>(30) Priority:</p> <p>(43) Date of application publication: 15.05.81</p> <p>(84) Designated contracting states:</p>	<p>(71) Applicant: MATSUSHITA ELECTRIC LTD</p> <p>(72) Inventor: TAKAGI YOSHIYUKI ISHIHARA TAKESHI</p> <p>(74) Representative:</p>
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(54) SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

(57) Abstract:

PURPOSE: To readily wire a multichip package by fixedly connecting a plurality of chips with an electrode leading pad connected to both front and back surface of a substrate through a penetrating conductive layer therebetween.

CONSTITUTION: An aluminum penetrating diffused layer 54 is, for example, formed in a substrate 51, and insulating film 55, integrated circuit 56, an electrode pickup pad 57 and a protecting film 58 are formed sequentially thereon. Further, an insulating film 55' and an electrode leading pad 57' are formed on the back surface of the substrate 51, and the pads 57 and 57' are conducted with aluminum and silicon eutectic crystal P type high density diffused layer. Such chips 51, 51a and 51b are formed in a laminate architecture, the

back surface pad 57' of the chip 51 and the surface pad 57a of the chip 51a are adhered with solder bump 60, the back surface pad 57a' of the chip 51 and the surface pad 57b of the chip 51b are adhered with solder bump 61, and the back surface pad 57b' of the chip 51b and the external lead 62 of the package are adhered with solder bump 63.

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